CLAIM AMENDMENTS

Please amend the claims as described herein below.

Claims 1-2 **(CANCELED).**

3**(CURRENTLY AMENDED).** A method of forming a package device, comprising;

providing a package substrate having a first side and a second side and having first pads on the first side and second pads on the second side;

placing a first integrated circuit on the first side and a second integrated circuit on a second side, wherein die attach material is interposed between the first integrated circuit and the second integrated circuit;

electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads; and

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads,

wherein at least one of the first pads is electrically independent of all of the second pads, and wherein ~~the~~ encapsulating material does not overlie at least one pad.

4**(ORIGINAL).** The method of claim 3, wherein the step of attaching is further characterized by:

the first integrated circuit being placed on the first side prior to the second integrated circuit being placed on the second side.

5(**ORIGINAL**). The method of claim 4, wherein the step of electrically connecting is further characterized by:

the first integrated circuit being electrically connected to the first pads prior to the second integrated circuit being electrically connected to the second pads.

6(**CURRENTLY AMENDED**). A method for forming a package device, comprising:

providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane, and wherein the package substrate has first pads on the first surface and has second pads on the second surface;

placing a first integrated circuit in the cavity;

placing a second integrated circuit adjacent to the first integrated circuit outside the cavity, such that die attach material is interposed between the first integrated circuit and the second integrated circuit; ~~and~~

depositing encapsulating material over the first integrated circuit and the second integrated circuit;

electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads; and

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads,

wherein at least one of the first pads is electrically independent of all of the second pads, and wherein the encapsulating material does not overlie at least one pad.

7(**ORIGINAL**). The method of claim 6, wherein the step of depositing comprises:

depositing a first portion of the encapsulating material over the first integrated circuit prior to the step of placing the second integrated circuit; and

depositing a second portion of the encapsulating material over the second integrated circuit.

8(**ORIGINAL**). The method of claim 7, further comprising:

placing a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material.

9(**CURRENTLY AMENDED**). The method of claim 6, wherein the package substrate further comprises ~~first pads on the first surface, second pads on the second surface,~~ first bond fingers on the first surface, and second bond fingers on the second surface~~, further comprising;~~

~~electrically connecting the first integrated circuit to the first pads;~~

~~electrically connecting the second integrated circuit to the second pads; and~~

~~testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads~~.

10(**ORIGINAL**). The method of claim 9, wherein the step of electrically connecting the first integrated circuit comprises wire bonding.

11(**ORIGINAL**). The method of claim 6, wherein the package substrate further comprises a supporting member along the second plane of the substrate.

12(**ORIGINAL**). The method of claim 11, wherein the supporting member is between the first integrated circuit and the second integrated circuit.

13(**ORIGINAL**). The method of claim 12, wherein the supporting member is electrically conductive.

14(**ORIGINAL**). The method of claim 11, further comprising removing the supporting member prior to step of placing the second integrated circuit.

15(**ORIGINAL**). The method of claim 14, wherein supporting member is tape.

Claims 16-27 (**CANCELED**)

28(**PREVIOUSLY PRESENTED**). The method of claim 7, wherein the step of depositing the first portion of the encapsulating material comprises transfer molding the encapsulating material, and wherein the step of depositing a second portion of the encapsulating material comprises transfer molding the encapsulating material.

29(**PREVIOUSLY PRESENTED**). The method of claim 8, wherein the third integrated circuit is stacked at least partially overlying at least one of the first and second integrated circuits.

30(**CURRENTLY AMENDED**). A method for forming a package device, comprising:

providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane;

placing a first integrated circuit in the cavity;

placing a second integrated circuit adjacent to the first integrated circuit outside the cavity, such that a supporting member is interposed between the first integrated circuit and the second integrated circuit; and

depositing encapsulating material over the first integrated circuit and the second integrated circuit,

wherein the package substrate is not formed from encapsulating material, and wherein the step of depositing comprises:

depositing a first portion of the encapsulating material over the first integrated circuit prior to the step of placing the second integrated circuit; and

depositing a second portion of the encapsulating material over the second integrated circuit,

wherein the method further comprises placing a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material.

31(**PREVIOUSLY PRESENTED**). The method of claim 30, wherein die attach material is interposed between the first integrated circuit and the second integrated circuit.

32(**PREVIOUSLY PRESENTED**). The method of claim 30, wherein the supporting member is electrically conductive.

33(**PREVIOUSLY PRESENTED**). The method of claim 30, further comprising removing the supporting member prior to step of placing the second integrated circuit.

34(**PREVIOUSLY PRESENTED**). The method of claim 30, wherein supporting member is tape.

35(**PREVIOUSLY PRESENTED**). The method of claim 30, further comprising:

electrically connecting the first integrated circuit to first pads, wherein the first pads are located on the first surface; and

electrically connecting the second integrated circuit to second pads, wherein the second pads are located on the second surface.

36(**PREVIOUSLY PRESENTED**). The method of claim 35, wherein the encapsulating material does not overlie at least one pad.

37(**PREVIOUSLY PRESENTED**). The method of claim 35, wherein the step of electrically connecting the first integrated circuit comprises wire bonding.

38(**PREVIOUSLY PRESENTED**). The method of claim 35, further comprising:

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads,

39(**CANCELED**).

40(**CURRENTLY AMENDED**). The method of claim ~~39~~ 30, wherein the step of depositing the first portion of the encapsulating material comprises transfer molding the encapsulating material, and wherein the step of depositing a second portion of the encapsulating material comprises transfer molding the encapsulating material.

41(**CANCELED**).

42(**CURRENTLY AMENDED**). The method of claim ~~41~~ 30, wherein the third integrated circuit is stacked at least partially overlying at least one of the first and second integrated circuits.

43(**CURRENTLY AMENDED**). A method for forming a package device, comprising:

providing a package substrate having a first side and a second side;

providing first pads on the first side;

providing second pads on the second side; ~~and~~

providing a first integrated circuit mounted to the package substrate;

providing a second integrated circuit mounted to the package substrate; and

providing a third integrated circuit adjacent to the second integrated circuit,

wherein the first integrated circuit is electrically connected to the first pads and the second integrated circuit is electrically connected to the second pads,

wherein the first pads and the second pads are further characterized as being useful for receiving test probes for testing, and

wherein one of the first and second ~~test~~ pads is not covered by an encapsulating material and is exposed for receiving one of the test probes.

44(**CANCELED**).

45(**CANCELED**).

46(**CURRENTLY AMENDED**). The method of claim ~~45~~ 43, wherein the substrate is further characterized as having a cavity and the first integrated circuit is further characterized as being in the cavity.

47(**PREVIOUSLY PRESENTED**). The method of claim 46, wherein the second integrated circuit is mounted to the substrate by adhesive die attach tape.

48(**PREVIOUSLY PRESENTED**). The method of claim 47, wherein the first integrated circuit is adjacent to the second integrated circuit.

49(**PREVIOUSLY PRESENTED**). The method of claim 48, further comprising providing a supporting member between the first integrated circuit and the second integrated circuit.

50(**PREVIOUSLY PRESENTED**). The method of claim 49, wherein the supporting member comprises die attach material.